NASA TECHNICAL NOTE

NASA TN D-2627

NASA TN D-2627

FLYBACK VOLTAGE REGULATOR

by Gail D. Smith

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • FEBRUARY 1965

FLYBACK VOLTAGE REGULATOR

By Gail D. Smith

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Office of Technical Services, Department of Commerce,
Washington, D.C. 20230 -- Price $1.00

FLYBACK VOLTAGE REGULATOR

by
Gail D. Smith
Goddard Space Flight Center

SUMMARY

The flyback voltage regulator provides a regulated output dc voltage from a widely varying input dc voltage to supply a widely varying output load. Its salient features are: good regulation, high efficiency, adjustable output voltage, constant frequency of operation, and rapid response to sudden changes in input voltage and output load.

The regulator employs the flyback phenomenon of an inductor to boost the input voltage and provide a regulated output voltage. A single high frequency, high power, low saturation resistance, switching transistor is used to connect the inductor in the charge and discharge or flyback circuits. A high speed, high gain, semiconductor feedback circuit detects changes in the output voltage and controls the charge and flyback times of the inductor to provide a regulated output voltage. The performance is shown by curves of the efficiency, ripple, and output voltage. These curves reveal the efficiency to be greater than 90 percent for a load of 60 to 100 percent of the maximum output power rating (44 watts) with an input of 12 to 20 volts.

CONTENTS

FLYBACK VOLTAGE REGULATOR

by
Gail D. Smith
Goddard Space Flight Center

INTRODUCTION

The design of satellite power systems frequently involves using an array of solar cells to charge a bank of batteries. The batteries provide power while the solar array is in partial or full shadow. Thus, the battery charge voltage may be double the minimum allowed discharge voltage, giving the satellite input voltage a two to one maximum to minimum ratio. Very few instruments can be operated on this widely varying voltage; consequently a voltage regulator is usually employed. In satellites bearing sensitive magnetic field detectors, stringent requirements are imposed on the effect the regulator has on the ambient magnetic field. The load on the regulator's output usually varies widely because of the various modes of operation of the experiments. In addition to these requirements, the regulator must be highly efficient, lightweight, reliable and must operate at a constant frequency.

The flyback voltage regulator provides a regulated output dc voltage from a widely varying input dc voltage to supply a widely varying output load. Its salient features are good regulation, high efficiency, adjustable output voltage, constant frequency of operation, and rapid response to sudden changes in input voltage and output load. The flyback phenomenon of an inductor is employed to boost the input voltage and to provide a regulated output voltage. This is accomplished by alternately connecting the inductor in parallel and in series with the input voltage source. While the inductor is connected in parallel, the energy flowing into it is stored in the field of its magnetic core; and when it is connected in series, the stored energy is released at an enhanced voltage and flows to the output load. This process of the release by an inductor of its stored energy is commonly called flyback; hence the name *flyback voltage regulator.*

SEQUENTIAL CIRCUIT DESCRIPTION

The schematic diagram of the flyback voltage regulator is shown in Figure 1 tracings of the voltage and current signals as a function of time, at various points of the circuit, are shown in Figure 2. Inductor L1 (Figure 1) is the flyback inductor from which the circuit gets its name. Transistor Q1 is employed as a fast switch to make the two inductor connections. Inductor L1 stores energy when transistor Q1 is on and releases its energy to the load when Q1 is off. During the flyback interval, the stored energy develops a voltage across L1 which is in series aiding the input voltage. Thus, the output voltage can be greater than the input voltage. The output voltage

is regulated by regulating the ratio of the on to off time of Q1. Turning and holding this transistor on and off and regulating the various intervals of time is explained by following the sequence of events in the circuit.

Assuming that the regulator of Figure 1 is operating within limits of input voltage and output power, then at time t1 transistor Q1 is on (Figure 2D). Current flows from the positive input through L1, N1 of T1, and Q1 to common or to the negative side of the input. This current establishes a small voltage across winding N1 of T1 which induces a voltage on each winding with dotted terminals positive. The voltage on winding N2 provides current through D4 and the emitter to base junction of Q1 to hold this transistor in saturation.

The clock pulse generator provides the reference frequency for the voltage regulator. It produces an approximately constant frequency symmetrical square wave across winding N5 of T2 (Figure 2A). Capacitor C3 and resistor R7 differentiate this signal to provide short duration spikes (Figure 2B). At time t2 the voltage at terminal 9 of T2 goes positive (Figure 2A) and presents a positive spike (Figure 2B) to Q5. This turns Q5 on momentarily, allowing current to flow through N1 of T3, Q5, R8, and N2 of T3. The current through winding N1 of T3 induces a positive voltage at each of the transformer's dotted terminals. The voltage developed across winding N2 passes current through R7, Q5, and R8 to hold Q5 on (Figure 2C). The voltage developed on winding N4 turns Q4 on and holds it on. The voltage across winding N5 turns Q6 on (Figure 2J) and it stays on of its own volition.

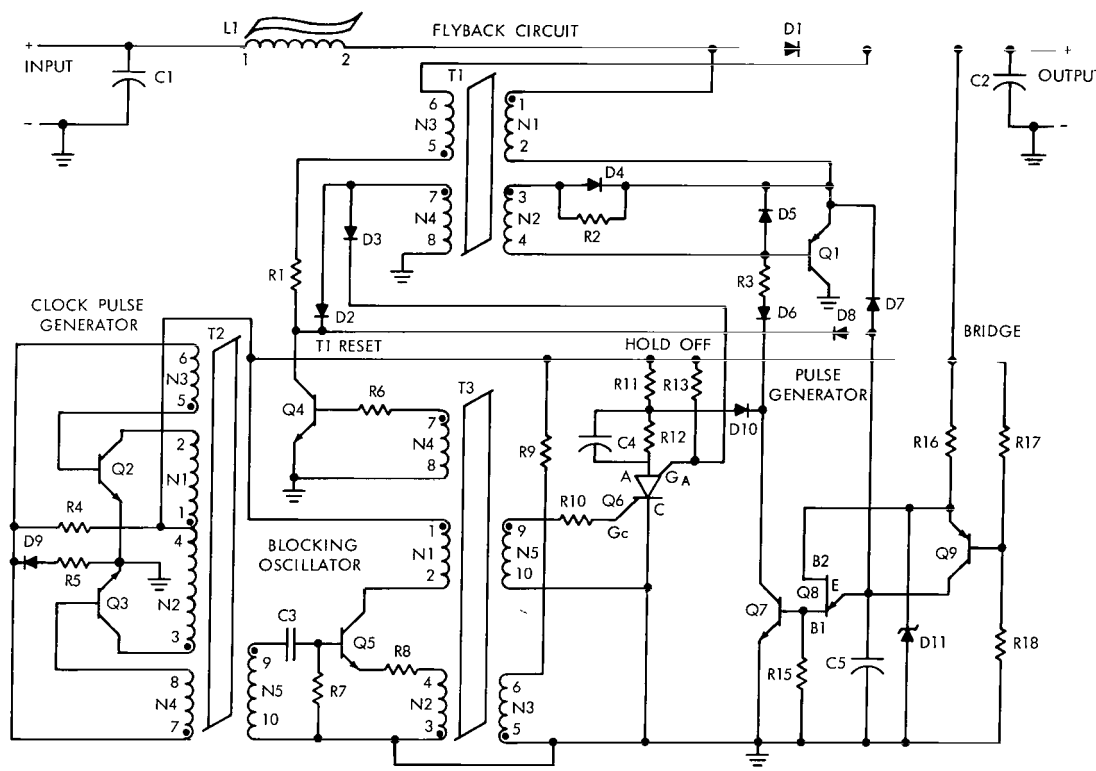

Figure 1—Flyback voltage regulator.

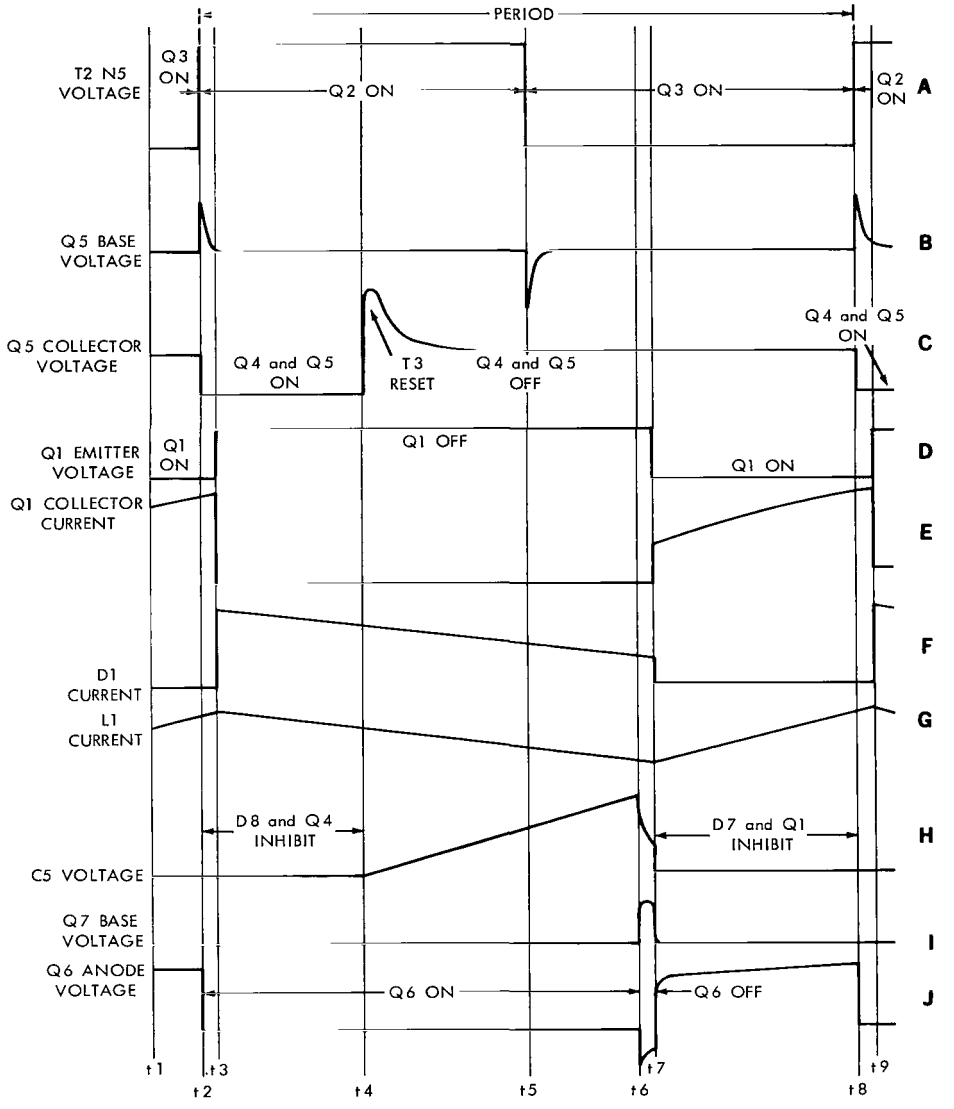

Figure 2–Wave forms.

When Q4 was turned on at time t2, C5 was inhibited from charging (Figure 2H) above about 2 volts by the low impedance path through D8 and Q4. A low impedance path is also established through D2 and Q4 for the positive voltage on terminal 7 of T1. This reduces the voltage on winding N4 of T1 to about 2 volts. The voltage then on winding N2 is about 0.1 volt. This reduces the bias on Q1 so that it almost goes off. With the reduced voltages on all windings of T1, the current flowing through N3 of T1, R1, and Q4 begins to reset this transformer. This current reverses the polarity of the T1 transformer voltages and turns Q1 off at time t3 (Figure 2D). The current continues to flow through winding N3 until T1 is reset to negative saturation. The current through winding N1 of T3 saturates this transformer at time t4 (Figure 2C). All transformer voltages collapse, thus

removing the hold on bias for Q5. This initiates the turn off of Q5. The resulting decrease in current through N1 causes all transformer voltages to reverse polarity. This turns off Q5 and Q4. The current flowing through R9 and N3 of T3 resets the transformer before the end of the period (Figure 2C).

When Q4 turned off at time t4, the T1 reset current was cut off. This decrease in current caused all T1 transformer voltages to reverse polarity, so that all dotted terminals are positive. The voltage on winding N2 tends to turn Q1 on; however, this transistor is held off by the Q6 hold off circuit. It is recalled that Q6 is on, having been turned on when Q5 and Q4 were turned on at time t2 (Figure 2J). Thus, a low impedance path is formed for a positive voltage on terminal 7 of T1 through D3 and Q6. This limits the positive voltage on N2 of T1, thus preventing Q1 from turning on.

When Q4 went off, the inhibit was removed from C5. Thus, this capacitor begins to charge (Figure 2H) at time t4. The rate of charge of C5 is a function of the regulator's output voltage via the bridge circuit. A fixed ratio of the output voltage which appears across R18 is compared with the reference voltage across the temperature compensated zener diode D11. The voltage difference is amplified by Q9 which also regulates the rate of charge of C5. Thus the rate at which C5 charges is related to the output voltage.

The unijunction transistor Q8 fires when C5 is charged to the peak point emitter voltage. That is, C5 discharges through Q8 at time t6 (Figure 2H). The resulting positive pulse at the base of Q7 (Figure 2I) is amplified and inverted to produce a negative spike at the collector of this transistor. This negative spike passes through D10 and C4 and swings the Q6 anode voltage negative (Figure 2J). The silicon controlled switch goes off, thus releasing the low impedance clamp on winding N4 of T1. Transformer T1 is now free to develop an on voltage for transistor Q1. The positive pulse at the base of Q7 turned this transistor on to saturation. The current flows from the input through L1, N1 of T1, Q1, R3, D6, and Q7. Transistor Q1 is turned on (Figure 2D) at time t 7 by this current and is held on by T1.

Capacitor C5 cannot charge above approximately 2 volts due to the low impedance path through D7 and Q1 (Figure 2H). Transistor Q1 remains on until the end of the period. At this time (t8), the clock pulse generator (Figure 2A) initiates the turn on of Q5, Q6, and Q4 and turn off of Q1 at t9 in the manner described for time t2 and t3.

FLYBACK CIRCUIT

The flyback circuit is the prime power controlling portion of the circuit in Figure 1. It consists of C1, L1, D1, C2, and Q1 with transformer T1 serving to control Q1. While transistor Q1 is on, inductor L1 is connected across the input through N1 of T1 and Q1. The impedance of transformer T1 is very low compared to that of inductor L1 and Q1 is operated in saturation. Therefore, a very large portion of the input voltage is across the inductor. The rate of change of current through the inductor is given by Lenz's law:

$$e = -L \frac{di}{dt} \quad . \tag{1}$$

Thus with constant inductance L and voltage e across the inductor, the current i increases linearly with time (Figure 2E and G). Deviation from a straight line usually indicates that Q1 is not saturated or L1 is beginning to saturate. A large portion of the energy passing into the inductor is stored in the magnetic field of the core. When Q1 is off, the core's magnetic flux Φ decreases and the inductor develops a voltage e according to Faraday's law,

$$e = -N \frac{d\Phi}{dt} \quad . \tag{2}$$

This relationship shows that the decreasing flux during the flyback interval produces a voltage of opposite polarity to that for increasing flux during the energizing interval. Therefore, the generated voltage is positive at terminal 2 and negative at terminal 1 of L1. This voltage source is in series with the input and is poled to aid the input voltage. Thus, the voltage at the anode of D1 is the sum of the magnitudes of these two voltage sources. This enhanced voltage passes through D1 to the output.

During the energizing interval with Q1 on, the loop equation is

$$E_{in} = L \frac{\Delta i_{on}}{\Delta t_{on}} + E_{T1} + E_{Q1} \quad , \tag{3}$$

where

E_{in} = input voltage,

L = inductance of L1,

Δi_{on} = change in current while Q1 is on,

Δt_{on} = time Q1 is on,

E_{T1} = voltage across N1 of T1, and

E_{Q1} = emitter to collector voltage of Q1.

Similarly for the flyback interval with Q1 off, the loop equation is

$$E_{in} - L \frac{\Delta i_{off}}{\Delta t_{off}} = E_{D1} + E_O \quad , \tag{4}$$

where

Δi_{off} = change in current while Q1 is off

Δt_{off} = time Q1 is off,

E_{D1} = voltage across D1, and

E_O = output voltage.

For constant input voltage and load,

$$\Delta i_{on} = -\Delta i_{off} , \tag{5}$$

as is shown in Figure 2G. Replacing Δi_{off} in Equation 4 with the negative equivalent of Δi_{on} of Equation 3, the following is obtained:

$$E_O = E_{in} - E_{D1} + \left(E_{in} - E_{T1} - E_{Q1}\right) \frac{\Delta t_{on}}{\Delta t_{off}} . \tag{6}$$

E_{T1} and E_{Q1} are small compared to E_{in} and may be neglected. Thus, Equation 6 can be written:

$$E_O \approx E_{in} + E_{in} \frac{\Delta t_{on}}{\Delta t_{off}} - E_{D1} \tag{7}$$

However, the period T is given by

$$T = \Delta t_{on} + \Delta t_{off} , \tag{8}$$

which enables Equation 7 to be written as

$$E_{in} \approx \left(E_O + E_{D1}\right) \frac{\Delta T_{off}}{T} . \tag{9}$$

The forward voltage drop E_{D1} across rectifier D1 depends upon the current through it; however, the change in this voltage drop is small compared to the output voltage. Thus for constant input voltage, Equation 7 reveals the output voltage to be directly proportional to the ratio of on to off time of Q1. This regulator operates at constant frequency or period T ; consequently, Equation 9 shows the off time to be directly proportional to the input voltage for a constant output voltage. These equations also reveal the on and off times to be independent of the output power except for small variations in E_{D1}, E_{T1}, and E_{Q1}.

An expression for the inductance required of inductor L1 is derived and illustrated in Reference 1. This inductor must be designed for close inductance tolerance over the entire range of inductor current, temperature, energizing time, and flyback time. Another design goal must be high efficiency or low core and wire losses at peak current and maximum frequency. The method of designing inductors reported in Reference 2 is applicable to this design problem. In fact, this method was derived for designing the inductor for this circuit. It involves selecting the smallest toroidal core which meets the requirements of inductance, quality factor, range of frequency, and inductance tolerance as a function of magnetizing force and temperature. Thus a small efficient inductor design is easily obtained. It is frequently imperative that a toroidal inductor be used for

such a high frequency power inductor. For satellites with sensitive magnetic field detectors, it is often desirable to use toroidal magnetic cores because of their small effect upon the magnetic field.

Capacitor C1 serves as a filter to reduce input transients and the variation in current required from the input voltage source. It is assumed that the variation in the inductor current shown in Figure 2G may be detrimental to the input power source and the resulting voltage ripple may affect the operation of the flyback circuit. An expression for the capacitance required to limit the input voltage ripple to 10 percent is derived in Reference 1.

Current passes through diode D1 to the output (Figure 2F) only while transistor Q1 is off. Therefore, capacitor C2 is required to store energy during this time and to provide load current during the Q1 on time when there is no current being supplied through diode D1. The equation for the capacitance required to filter the output to 5 percent ripple voltage is derived in Reference 1. The equations for C1 and C2 must be satisfied throughout the operating temperature range; consequently the change in capacitance with the temperature should be taken into consideration. The type of capacitors used should have very low internal resistance to minimize power loss and self-heating.

The rectifying diode D1 allows current to flow to the output while Q1 is off and impedes current flow from the output through D1, T1 and Q1 while Q1 is on. A fast recovery, low leakage, high current silicon rectifier is used for D1. The power loss in this rectifying element is rather high, primarily due to the high forward voltage drop. High power switching transistors are sometimes suitable for this type of application because of the low forward voltage drop. However, the power loss due to greater reverse leakage and longer recovery time approximately negates the power saved at frequencies above a few kilocycles per second. The current spikes which occur during the recovery time represent considerable power. Fast recovery diodes are used to minimize power loss due to current spikes.

Transistor Q1 functions as a switch. Thus, a low saturation resistance, high frequency, low leakage transistor is used. The dc and ac current gains must be high over the entire operating temperature range to enable the use of low power control circuitry.

Transformer T1 is employed to control transistor Q1. This is a toroidal transformer using a small, low-loss rectangular hysteresis loop core. The current flowing through N1 when Q1 is on develops a small voltage across this winding. To insure low loss, the minimum number of turns of heavy wire needed to achieve good magnetic flux coupling to the core is used. The voltage developed across winding N2 provides the base current to hold Q1 on. Neglecting losses, the ratio of Q1 collector current to base current is equal to the turns ratio of N2 to N1. This turns ratio must be less than the minimum dc current gain of transistor Q1 for all conditions of collector current and temperature. Winding N4 of this transformer is employed to hold transistor Q1 off. The Q1 leakage current through winding N1 induces a voltage on all transformer windings with the dotted terminals positive. At this time Q6 is

conducting, thus imposing a low impedance path through D3 and Q6 for the positive voltage on terminal 7 of T1. This limits the voltage on N4 to approximately 2 volts. With a N4 to N2 turns ratio of 20 to 1, the voltage across N2 is limited to approximately 0.1 volt; hence, Q1 is held off.

Winding N3 is employed to reset T1. Current reset is used; therefore, a high voltage spike developes initially across this winding. The induced voltage spike on winding N2 exceeds the reverse emitter base voltage rating of many transistors which are suitable for Q1. Diode D5 is employed to reduce the emitter base voltage on Q1 while T1 is being reset. Diodes D2 and D3 must have the following features to prevent the induced voltage on N4 from damaging them or transistors Q4 and Q6: fast-recovery, low-leakage, and high-voltage rating.

CLOCK PULSE GENERATOR

A Royer converter (Reference 3) is used as a clock pulse generator (Figure 1). Its signal (Figure 2A) serves as the basic frequency reference for the regulator. The frequency of oscillation is proportional to the supply voltage, which is the regulator's output voltage. Thus, frequency regulation is obtained through supply voltage regulation.

During half of the period, transistor Q2 is on with Q3 off and for the other half, Q3 is on with Q2 off (Figure 2A). While Q2 is on, to saturation, its collector to emitter voltage is very low; consequently, most of the supply voltage is across winding N1 of T2. A voltage is induced on all other transformer windings with the dotted terminals positive. The voltage on winding N3 provides base current through R5 and D9 to hold Q2 on. The voltage on winding N4 holds Q3 off. Transistor Q2 remains on until the rectangular hysteresis loop core of transformer T2 saturates. At this time all transformer voltages collapse. Transistor Q2 remains on due to its storage, and its collector current increases momentarily because of the reduced impedance of the transformer. After the storage time, Q2 collector current and T2 magnetic flux begin to decrease. The decreasing flux induces a voltage of opposite polarity (Equation 2) on all windings. This turns Q2 off and Q3 on. These two transistors remain in this state of conduction until the transformer core saturates in the negative direction. At this time the states of conduction are reversed and oscillation continues.

Initiation of oscillation is accomplished through resistor R4. The oscillation initiates the flyback action which boosts the regulator's output voltage; therefore, the CPG must start on the unboosted voltage. Starting current flows from the input through L1, D1, R4, N3 of T2 and Q2 and through a parallel path consisting of N4 of T2 and Q3. This means that oscillation must start with a supply voltage somewhat lower than the minimum input voltage. Diode D9 blocks current flow from the supply voltage through R4, D9, and R5. Resistor R5 limits the Q2 and Q3 forward base current.

Transformer T2 is designed to cycle from positive flux saturation (Φ_m) to negative flux saturation $(-\Phi_m)$ in one half period $(T/2)$. The voltage drop due to resistance of the transformer

winding and the collector-to-emitter voltage of the transistor are negligible compared to the supply or output voltage E_O. The rate of change of the magnetic flux in the transformer core is given by

$$E_O = 10^{-8} N_1 \frac{d\Phi}{dt} \quad . \tag{10}$$

where

E_O = output voltage in volts,

N_1 = number of turns of wire for N1 of T2,

Φ = magnetic flux in maxwells, and

t = time in seconds.

By writing this in integral form for a half period,

$$E_O \int_O^{\frac{T}{2}} dt = 10^{-8} N_1 \int_{-\Phi_m}^{+\Phi_m} d\Phi \quad . \tag{11}$$

Integration of Equation 11 gives

$$E_O \frac{T}{2} = 10^{-8} N_1 \; 2\Phi m \quad . \tag{12}$$

It is known that

$$T = \frac{1}{f} \tag{13}$$

and

$$\Phi_m = B_m A \quad , \tag{14}$$

where

T = period in seconds,

f = frequency in cycles per second,

B_m = maximum magnetic flux density in gauss, and

A = cross-sectional area of the core in square centimeters.

Inserting Equations 13 and 14 into Equation 12 yields

$$E_O = (4)\ 10^{-8}\ N_1 B_m A f \quad . \tag{15}$$

Equation 15 is employed to design transformer T2 where E_O and f are given, B_m and A are constants of the selected core and N_1 is to be determined.

BLOCKING OSCILLATOR

The blocking oscillator controls the time the reset signal is applied to T1 through Q4 and initiates the Q6 hold-off circuit. The square wave (Figure 2A) produced by the clock pulse generator across winding N5 of T2 is differentiated (Figure 2B) by C3 and R7. The positive spike on the base of Q5 at time t2 turns this transistor on momentarily. Current then flows from the regulator's output through N1 of T3, Q5, R8, and N2 of T3. The major portion of this voltage is across N1 of T3; therefore, the voltage induced on all other T3 windings is positive at the dotted terminals. The voltage induced on winding N2 provides base current for Q5 through R7, Q5, and R8, to hold this transistor on to saturation. Thus Q5 remains on after the initiating spike disappears. The voltage on winding N4 holds transistor Q4 on. Transistors Q4 and Q5 are held on by transformer T3; therefore they turn on and off simultaneously. The voltage on winding N5 turns Q6 on, which remains on due to a self-clamping action. Transistor Q5 remains on until the rectangular hysteresis loop core of transformer T3 saturates. At this time all transformer voltages collapse. Transistor Q5 remains on momentarily due to its own and external energy storage. As the collector current and T3 magnetizing force decrease, the polarity of all transformer voltages reverse and turn Q4 and Q5 off. The on time of Q4 and Q5 (see Equation 11) is the time required for the core of T3 to go from negative to positive flux saturation. Thus, the number of turns for winding N1 is computed using Equation 12 by replacing T/2 with the Q5 on time.

After Q5 goes off, the current through R9 and N3 of T3 resets this transformer to negative saturation. The core remains in negative saturation until Q5 is turned on at the beginning of the next period.

TRANSFORMER T1 RESET CIRCUIT

The blocking oscillator turns transistor Q4 on, thus allowing current to flow from the regulator output through N3 of T1, R1 and Q4 to reset T1. The interval of time this current is allowed to flow through the T1 reset winding is determined by the design of the blocking oscillator transformer (T3). Sufficient time must be allowed to insure complete reset action under all conditions of operation.

BRIDGE

The bridge circuit serves to detect and amplify changes in the output voltage and to charge capacitor C5 at a rate which is inversely proportional to the output voltage. The temperature compensated zener diode D11 is employed as a voltage reference. A fixed ratio of the output voltage appearing across R18 is compared with the reference voltage by transistor Q9. This transistor amplifies the error signal and controls the charging rate of capacitor C5. The current through D11 is determined primarily by the resistance of R16. This resistance is computed to allow sufficient, but not excessive, current flow to insure a minimum possible change in the reference voltage for all conditions of output voltage and temperature.

PULSE GENERATOR

The pulse generator serves to turn Q6 off and Q1 on. When capacitor C5 is charged to the peak point emitter voltage of the unijunction transistor Q8, the emitter becomes forward biased. The dynamic resistance drops to a low value and discharges capacitor C5 through Q8 and Q7. The positive pulse at base-one of Q7 is amplified, inverted, and appears as a negative pulse at the collector. This pulse passes through D10 and C4 and turns Q6 off. It is recalled that when Q6 was on, it formed a low impedance shunt for a positive voltage on the dotted terminals of T1. This was to prevent Q1 from being turned on by T1. Therefore Q6 must go off before Q1 can be held on by T1. While Q7 is on, current flows from the input through L1, N1 of T1, Q1, R3, D6 and Q7. The resistance of resistor R3 is calculated to insure that this current turns Q1 on to saturation. After Q6 goes off, the voltage across winding N1 induces a voltage on all other windings with the dotted terminals positive. The voltage across winding N2 then holds Q1 on. It is observed that Q7 and Q8 must remain on sufficiently long for Q6 to go off and for T1 to clamp Q1 on. The on time of these two transistors is the time required to discharge C5 from the peak to valley point voltage of Q8.

HOLD-OFF CIRCUIT

The hold-off circuit holds the main power controlling transistor Q1 off during the T1 reset and C5 charge times. The blocking oscillator produces a positive voltage at terminal 9 of T3 winding N5 during the reset interval. This positive signal at the cathode gate (Gc) turns the silicon controlled switch Q6 on. The SCS remains on due to the anode hold-on current through R11 and R12. Thus the total resistance of these two resistors is calculated to insure sufficient hold-on current over the entire range of operating temperature. While this SCS remains on, the impedance of D3 and Q6 for a positive voltage at terminal 7 of T1 is very low. In fact, the voltage on this transformer winding is not able to exceed approximately 2 volts. This transformer is designed to limit the voltage on winding N2 to approximately 0.1 volt. Thus, transistor Q1 cannot be held on by T1 while Q6 is on.

When capacitor C5 is charged to the peak point emitter voltage of Q8, the pulse generator produces a negative pulse at the collector of Q7. This pulse passes through D10 and C4 and swings the anode of Q6 negative. The anode hold-on current is thereby cut off momentarily and Q6 goes off. Transformer T1 is then able to develop a positive voltage at the dotted terminals to hold transistor Q1 on.

TEST RESULTS

The performance of the flyback voltage regulator which was designed, constructed, and tested, is shown in Figures 3, 4, and 5. This regulator was designed to operate on an input of 12 to 20 volts and to provide a regulated voltage with an output power of 22 to 44 watts. The clock pulse generator frequency was approximately 1500 cycles per second. The efficiency as a function of output power for an input of 12, 16, and 20 volts is shown in Figure 3. It is observed that the data was taken to 25 percent of maximum output power instead of the required 50 percent. These curves reveal the efficiency to be 91.4 to 94 percent for an output power of 44 watts, 89.8 to 94 percent for 22 to 44 watts, and 86.6 to 94 percent for 11 to 44 watts. Regulation of the output voltage is shown in Figure 4. This shows the output voltage as a function of output power for three different input voltages. These curves reveal the output regulation to be ±1.1 percent. Figure 5 indicates the output ripple as a function of output power for an input of 12, 16, and 20 volts. The maximum ripple is 260 millivolts peak to peak.

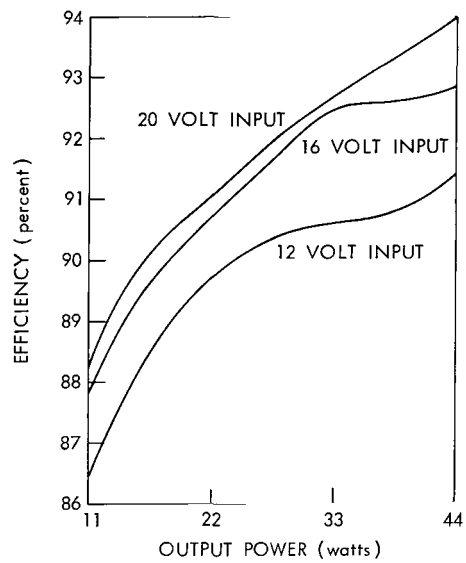

Figure 3–Efficiency versus power output.

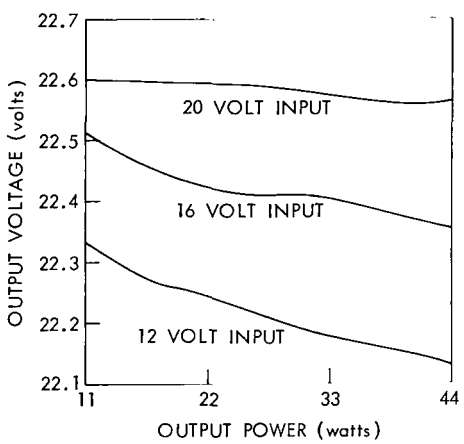

Figure 4–Output voltage versus output power.

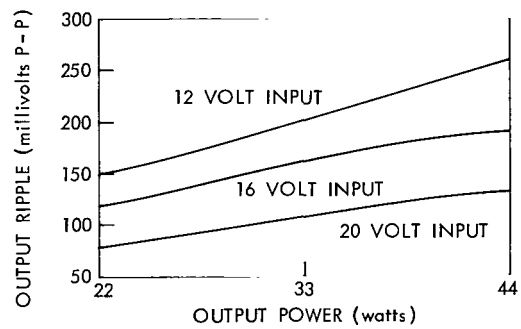

Figure 5–Output ripple versus output power.

(Manuscript received August 31, 1964)

REFERENCES

1. General Electric Company's Direct Energy Conversion Operation, "Voltage Regulation and Conversion in Unconventional Electrical Generator Systems," Quarterly Report Numbers 1 and 2 combined, July 30, 1962.
2. Smith, G. D., "Designing Toroidal Inductors with DC Bias," NASA Technical Note D-2320, June 1964.
3. Royer, G. H., "A Switching Transistor DC to AC Converter Having an Output Frequency Proportional to the DC Input Voltage," in: *AIEE Transactions Part I, Communications and Electronics*, pp. 322-324, July 1955.

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Technical information generated in connection with a NASA contract or grant and released under NASA auspices.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

TECHNICAL REPRINTS: Information derived from NASA activities and initially published in the form of journal articles.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities but not necessarily reporting the results of individual NASA-programmed scientific efforts. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546